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Application Note

ADVANTAGES AND APPLICATION OF DISPLAY INTEGRATING A/D CONVERTERS

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Introduction

In making basic bridge and dc measurements, the integrating A/D converter has become the workhorse for many significant reasons. While cost and the availability of architectures with built in display drivers are certainly among them, the advantage of the integrating converter is its relative immunity to noise that is synchronous with the integrating period, both common and normal mode, and the fact that a true integrator features no missing codes. The purpose of this paper is to acquaint the user with some of the basic idiosyncracies of the popular A/D architectures and to demonstrate why the integrating format is the preferred format for dc and low frequency (generally <1Hz) measurements.

Popular A/D Architectures

One of the major limitations of any A/D system is noise. Aside from any uniquely generated internal noise, the system also has to deal with noise that is both common mode (common to both inputs) and normal mode (unwanted noise appearing in series with, or across the input terminals.) A/D's using the successive approximation algorithm (SAR) can't really deal with either. The algorithm only tells the user that the value measured was indeed present sometime during the conversion cycle.

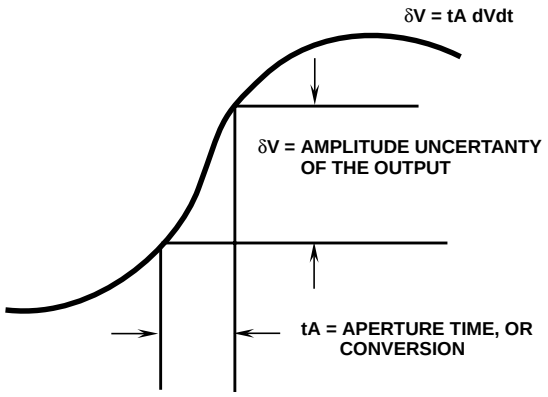


FIGURE 1. APERTURE TIME AND AMPLITUDE UNCERTAINTY

As shown in Figure 1, the width of the conversion window limits the useful bandwidth of the input signal but, as the result of the conversion can be any value of δV portrayed in the interval t_A. The result may well be an interpretation of an input noise pulse that can lead to a non-meaningful answer. One alternative is to use a sample and hold in front of the converter. While this will improve input bandwidth, which is just the opposite effect we were looking for, it would also pass through any noise pulse that does not average to zero during the acquisition period. Thus, for normal mode rejection, the user will have to provide an independent input amplifier configuration that will limit the input bandwidth as there is no inherent immunity in the SAR architecture. Finally unlike the integrating A/D, the SAR is not inherently monotonic, In fact simply testing the converter at the major carry's for 1/2 LSB does not necessarily guarantee the device will have no missing codes either. There is always some interaction along the transfer curve, and aging can cause many a converter to drift out of specification.

The Flash Converter

A flash converter is considered the epitome in gaining accurate measurement of high speed events. In general the user is trying to look at all aspects of the input signal and hence will use front end analog filters to eliminate aliasing errors or DSP techniques on the digital output if it is appropriate to filter out known sources of noise, or to create other high pass, low pass, bandpass characteristics. While many flash converters feature internal sample hold functions, they frequently present a non-trivial capacitive load to the source and the user has to take some bold steps to compensate the amplifier.

The basic architecture of a full flash converter uses one comparator for every bit, with the comparators stacked on top of each other on a continuous ladder. The result of such a conversion is frequently called a thermometer code, which is subsequently decoded to produce its binary equivalent. On the surface one would believe that the system is inherently monotonic; and designers go to great lengths to try to achieve it, starting with auto zeroed comparators such as those found in the HI5700 and HI5701. But timing and routing of internal components can make or break the design. In the case of HI5700 and HI5701 significant effort went into the design of the comparators to insure quick settling and

recovery from overload, to eliminate the 'sparkle code' phenomena that leads to non-monotonic operation. And while the cost of flash converters has come down considerably over the past few years it is clearly overkill to use this architecture to measure dc events, and it has virtually no ability to filter out common mode noise. Normal mode noise would require a sophisticated DSP filter, but as the flash architecture is frequently used to capture these mysterious events it's simply a case of using the wrong converter for the job.

The Integrating Converter

The integrating converter offers the designer several unique advantages. First, the converter is monotonic (no missing codes) by definition. Integrators can become very nonlinear, but this writer has never seen one whose second derivative changed sign! Second, choosing the period of integration to be a multiple of the powerline period will virtually eliminate normal mode noise (noise appearing in series with the input) at the powerline frequency when making dc measurements. As depicted in Figure 2, this is a major advantage of the integrating architecture as the integrator behaves as a virtual band reject filter for frequencies whose periods are multiples of the integrating period and as a low pass filter for all others. Though not necessarily inherent in the integrating architecture, (or any other conversion architecture, for that matter), excellent common mode rejection can be achieved with careful chip design and layout. And finally, many versions come complete with an LED or LCD display driver, such as HI7131 and HI7133. The functional diagram of an integrating converter is shown in Figure 3.

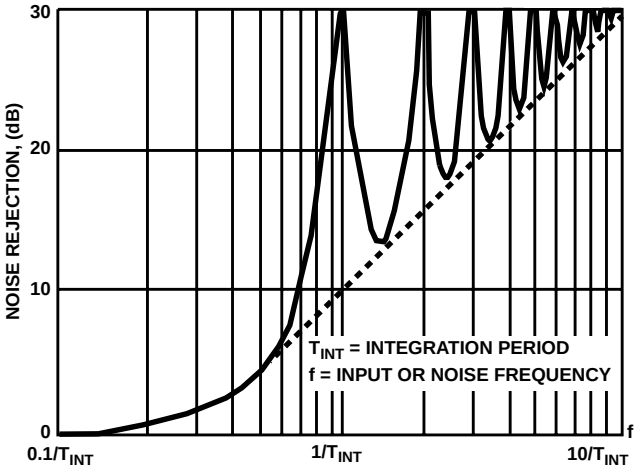
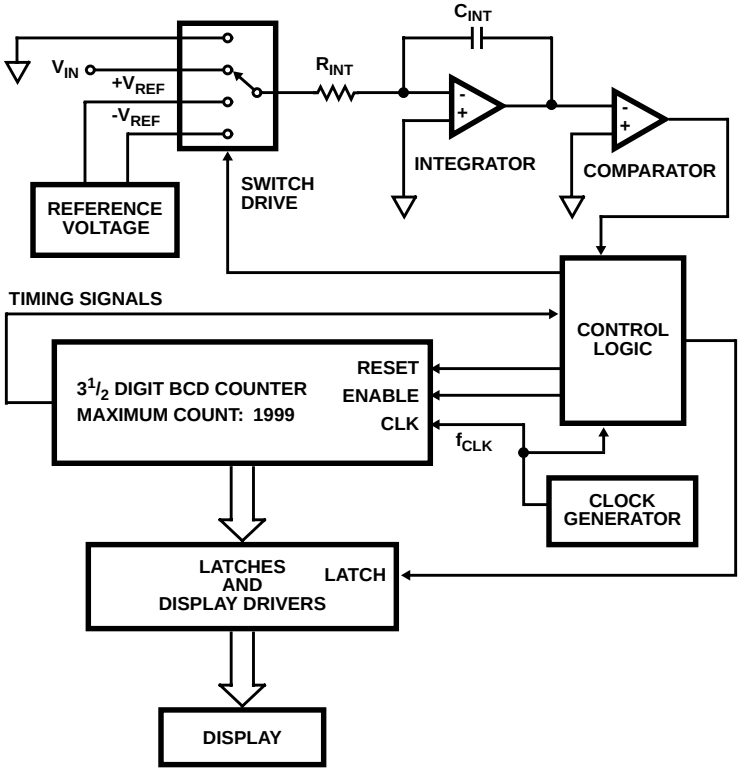
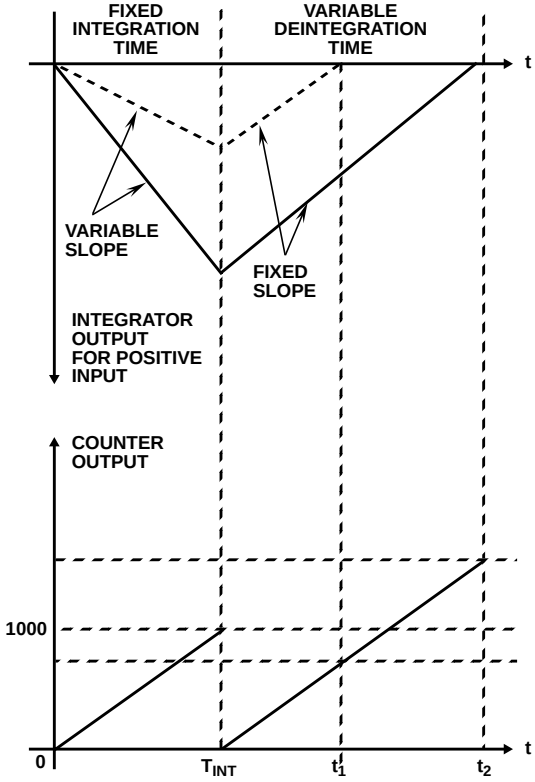


FIGURE 2. NORMAL MODE REJECTION OF AN INTEGRATING CONVERTER AS A FUNCTION OF FREQUENCY





$$AV_{INT} = \frac{I}{H_{INT}C_{INT}} \int_0^{T_{INT}} V_{IN} = \frac{I}{R_{INT}C_{INT}} \int_0^{T_{DEINT}} V_{REF}$$

$$AV_{INT} = \frac{\overline{V_{INT}}T_{INT}}{R_{INT}C_{INT}} = \frac{V_{REF}I_{DEINT}}{R_{INT}C_{INT}}$$

$\overline{V_{IN}}$ = INPUT AVERAGE DURING INTEGRATION

$$T_{INT} = 1000\left(\frac{I}{I_{CLK}}\right)$$

$$I_{DEINT} = \text{ACCUMULATED COUNTS}\left(\frac{I}{I_{CLK}}\right)$$

$$\text{ACCUMULATED COUNTS} = 1000\frac{\overline{V_{IN}}}{V_{REF}} = \text{DISPLAY READING}$$

FIGURE 3. DUAL SLOPE INTEGRATING A/D CONVERTER

A complex switch configuration at the front end is required to alternately short the input terminals to “COMMON” during the autozero phase, to the source during the integrate phase, and to the reference during the de-integrate phase. As will be shown later, these converters generally feature a differential input, and the polarity of the reference (which way it is connected between the differential inputs) is determined by the sign of the input signal. Using the same reference (and not just an inverter) assures greater accuracy when using this common reference in bridge type (radiometric) measurements.

Auto-Zero Phase

During this phase the inputs are shorted to common and fed, differentially, to the integrator configured in an autozero loop with a comparator.

The comparator (now inside the feedback loop) places incremental charges onto C_{AZ} until the output no longer changes. The reference capacitor, C_{REF}, is charged to the reference voltage.

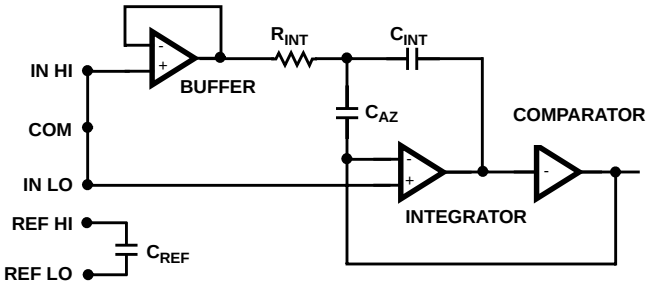


FIGURE 4. AUTOZERO PHASE

Signal Integrate Phase

In this phase the converter integrates the differential voltage between INHI and INLO for a fixed period of time, generally selected to be a multiple of the powerline frequency to optimize normal mode rejection.

For HI7133 this differential voltage can be within a wide common mode range (within 1 volt of either supply). At the end of this phase the polarity of the integrated signal is determined for use in the next phase.

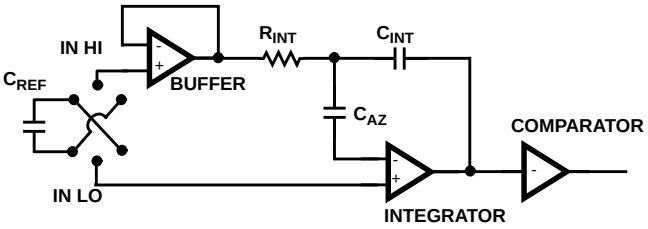


FIGURE 5. SIGNAL INTEGRATE PHASE

De-Integrate Phase

In this final phase the input to the integrator is connected across the previously charged reference capacitor, C_{REF} .

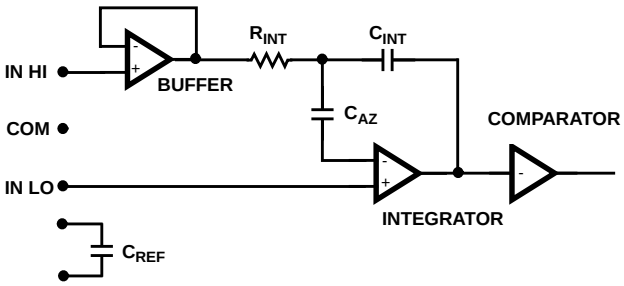


FIGURE 6. DEINTEGRATE PHASE

Internal logic senses the polarity of the integrated signal from the previous phase to insure the capacitor is connected in such a way that the integrator input will be driven toward zero. The time required for the output of the integrator to cross zero is then proportional to the input signal. For the 3-1/2 digit HI7133 A/D Converter that translates specifically to

$$1,000\left(\frac{V_{IMP}}{V_{REF}}\right)$$

Optimizing CMRR

One of the interesting vagaries of the integrating architecture is how to optimize CMRR in the presence of an architecture that provides for differential input, and differential reference with separable analog and digital ground references. Manufacturers also have some options that can lead to improved performance under certain conditions.

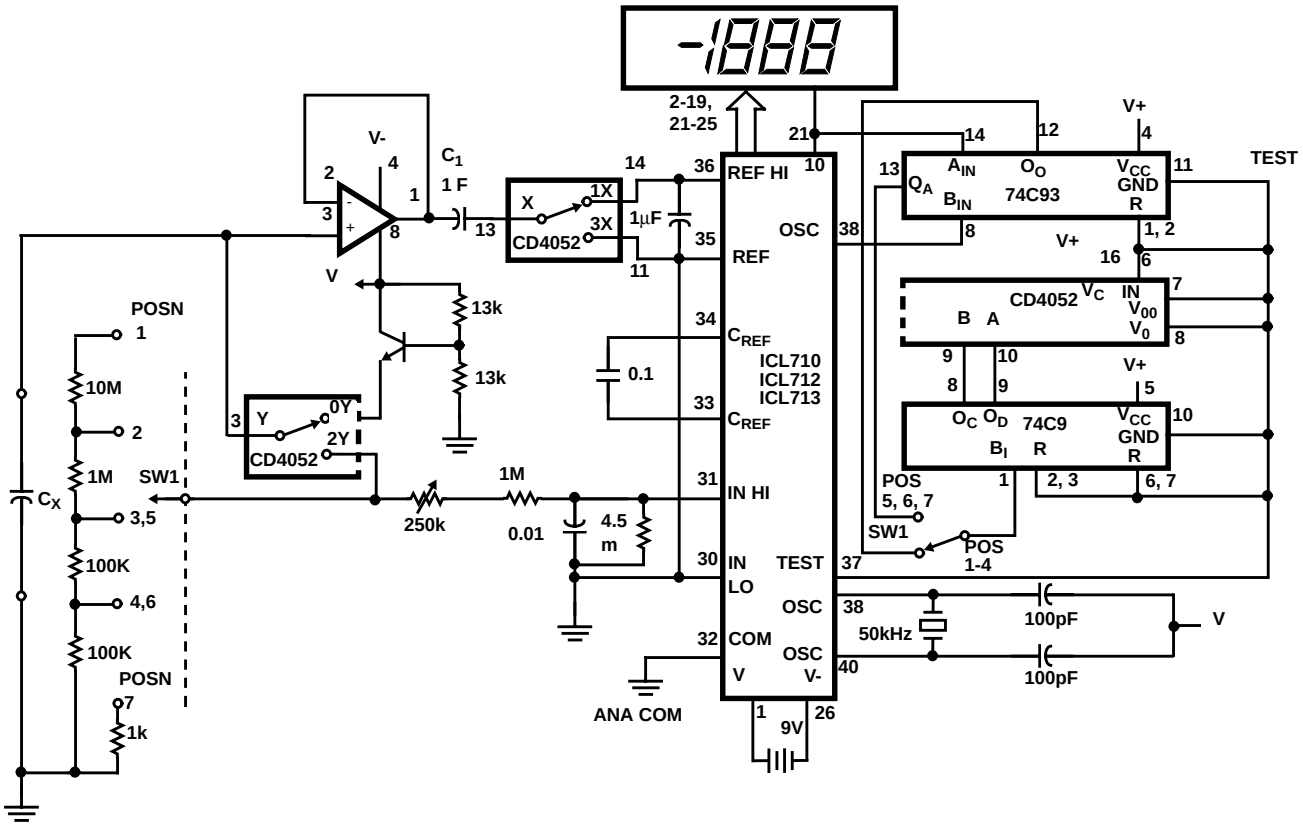
One such combination compares HI7133 with ICL7137. The basic difference is simply that INLO is ALWAYS connected to the non-inverting input of the integrator in the HI7133. In the case of ICL7137 the non-inverting input to the integrator uses INLO as a reference only during the integrate phase and COMMON during the autozero and de-integrate periods.

The approach used in HI7133 works very well for DC common mode errors, and for those in sync with the integration period, which is normally multiples of the power line, as users tend to select the integration period to optimize normal rejection at the power line frequency. Thus for designing panel meters that will be used in basic bridge and dc measurements (temperature, pressure, flow, volts, amperes, etc.) in the presence of dc or powerline related common mode noise HI7133 will provide improved CMR performance over the standard ICL7137. However, if non-synchronous CMV noise can be a significant factor users may find ICL7137 to be the better choice.

Applications

Integrating A/D Converters with on-chip display drivers are ideally suited for the construction of Digital MultiMeters (DMM) for classical Volt-Ohm measurements, or as an integral part of closed loop systems, such as flow meters, weigh/counting scales, digital thermometers etc.

A simple capacitance meter is depicted in Figure 7.



	SWITCH 1A	SWITCH 1B	MAXx C	COUNTER/SWITCH PHASES		
1	10M	6kHz	200pF	0Y	00	Charge C_X
2	1M	6kHz	2nF	1Y	01	V_{CX} on C_{REF}
3	100k	6kHz	20nF	2Y	10	Discharge C_X thru R_{net}
4	10k	6kHz	0.2 F	3Y	11	Reset C_t to zero
5	100k	60kHz	2 F			
6	10k	60kHz	20 F			
7	1k	60kHz	200 F			

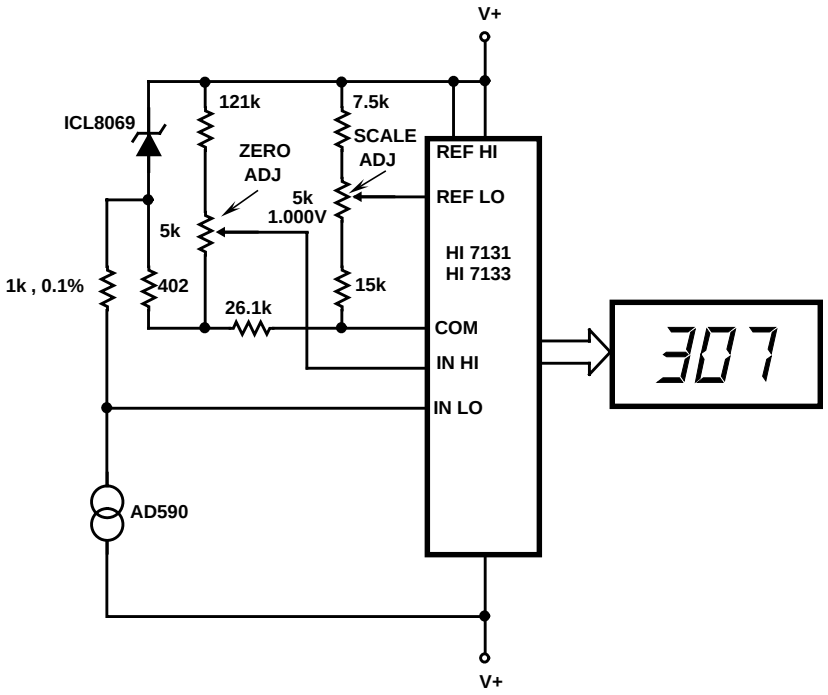
FIGURE 7. CAPACITANCE METER (200pf to 200 F)

Designed to measure capacitance in the range 200 pF to 200 F, the circuit works by alternately charging and discharging the capacitor at a crystal controlled rate and stores the change in voltage on a sample- difference amplifier. The current that flows during the discharge cycle is averaged and measured ratiometrically in the A/D using the voltage change as the reference.

A temperature measurement circuit, with zero adjust, is shown in Figure 8. Using the Intersil AD590 two-wire current output temperature transducer with HI7131 or HI7133, the user can adjust the circuit to achieve a direct reading in degrees Kelvin or Fahrenheit. This circuit allows “zero adjustment” as well as slope adjustment. The ICL8069 precision reference brings the input within the common mode range, while the 5k potentiometers trim any offset at 218 K (-55 C), and sets the scale factor.

Multirange voltage and current measurements are shown in Figure 9A and 9B, respectively. For measuring resistance, (Figure 9C), the unknown resistor is put in series with a known standard and a current is passed through the pair. The voltage developed across the unknown is applied to the input terminals while the voltage developed across the standard resistance is applied to the reference input. The displayed reading can be determined from the following expression,

$$\text{Display Reading} = \frac{R_{Unknown}}{R_{Known}} \times 1,000$$



SCALE	V_{IN} RANGE (V)	R_{INT}(k)	C_{AZ}(F)
K	0.223 to 0.473	220	0.47
C	-.25 to +1.0	220	0.1
F	-0.29 to +0.996	220	0.1

FIGURE 8. BASIC DIGITAL THERMOMETER

Guidelines for Using Integrators

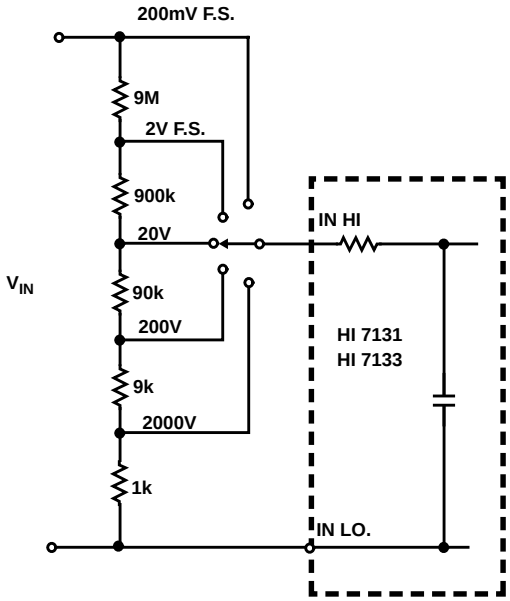
1. Plan grounding carefully. Keep separate grounds for digital and analog signals, and connect only back at the supply.
2. Plan layout very carefully. Keep oscillator and digital signal and timing traces away from analog signal paths. If space is an issue isolate the analog paths from timing and digital paths using ground planes, guard rings and/or traces. Particularly watch for capacitive coupling to the reference, autozero and integrating capacitors.
3. While component selection is generally not critical for integrating converters, dielectric absorption in the integrating autozero and reference capacitor is, and the integrating resistor must have negligible voltage coefficient to ensure linearity.
4. If possible include any input signal conditioning or instrumentation amplifier in the autozero loop. Many integrating converters provide a digital control signal for just such a purpose.
5. Tie unused digital inputs up to vt (or down to the test pin) if not in use. This will reduce noise due to unwanted spikes.
6. Bypass all supplies with a large and small capacitor close to the device package.
7. Guard against stray paths that can either result in dc leakage currents or capacitive coupling into sensitive low level analog signals.

Bibliography:

A002 Principles of Data Acquisition and Conversion (Intersil Applications Handbook 1988)

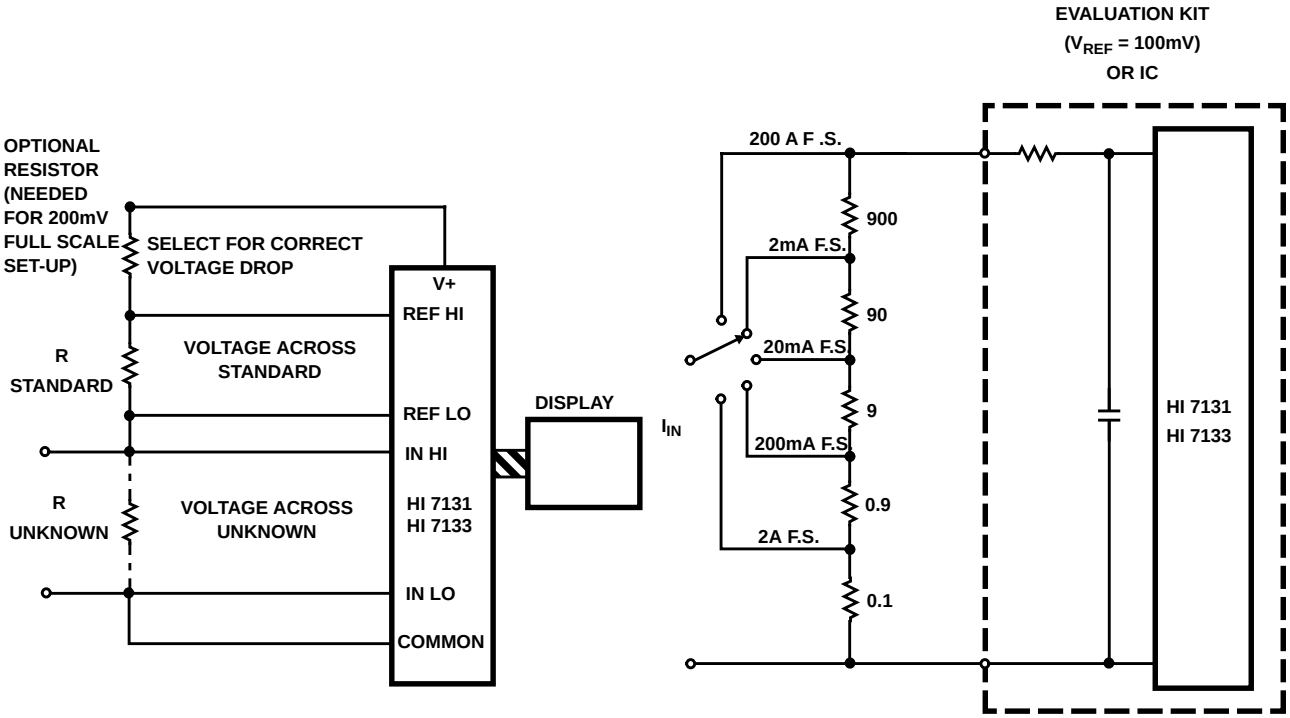
A016 Selecting A/D Converters (Intersil Applications Handbook 1988)

A047 Games People Play with Intersil's A/D Converters (Intersil Applications Handbook 1988) ?



CAUTION: HIGH VOLTAGES CAN BE LETHAL. PROPER OPERATING PRECAUTIONS MUST BE OBSERVED BY THE USER. INTERSIL ASSUMES NO LIABILITY FOR UNSAFE OPERATION.

(A) MULTIRANGE VOLTMETER



B) RESISTANCE MEASUREMENTS. THE OPTIONAL RESISTOR CAN BE REPLACED BY A DIODE STRING

(C) MULTIRANGE CURRENT METER

FIGURE 9. DVM CIRCUITS. VOLTAGE AND CURRENT MEASUREMENTS FOR METERING. FOR AUTO-RANGING CIRCUITS SEE A046 FOR THE 3-1/2 DIGIT DEVICES, AND A028 FOR THE 4-1/2 DIGIT PARTS.